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Formation of Shallow n-p Junctions in Cz-Si by Low-Energy Implantation of Carbon Ions

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A low-temperature method for shallow n-p junction formation in thin subsurface layers of p-type Cz-Si wafers is presented. Junctions are formed due to the enhanced formation of thermal donor centers by C ion implantation. It is shown that by C ion implantation with doses between 0.6 and 1.0×10^{14} cm^{-2} and subsequent annealing at temperatures in the range between 600 and 650 °C, n-p junctions with breakdown voltages of 100 to 150 V and reverse currents below 1×10^{-10} A at 20 V bias, can be formed. The highest breakdown voltages and lowest leakage currents were obtained for a C ion implantation dose of $1x10^{14}$ cm^{-2} and for annealing at 600 °C.

Introduction

As it is well-known, heat treatments of Czochralski grown (Cz-)Si in the temperature range between 400 and 1200 °C, result in the aggregation of the supersaturated interstitial oxygen O_i, leading to the formation of bulk defects (1,2). At temperatures between 450 and 650 °C, small oxygen clusters (O_3, O_4) grow and lead to the formation of shallow donor centers (3,4). The presence of substitutional carbon C_s atoms has an important impact on oxygen precipitation and the associated defect formation processes (5,7). The much smaller covalent radius R_c (= 0.077 nm) of the C atom compared to the Si lattice atom (R_c = 0.117 nm), causes tensile stress around the C_s atoms and influences the process of thermal donor formation (8). It was shown (9), that for samples with a low C_S content, double-charged thermal donors (DTDs) are created during thermal annealing between 400 and 550 °C, with a maximum concentration of about 10^{16} cm^{-3}, and single charged thermal donor centers (STDs) with an activation energy E_i of about 32 meV. In the samples with a high C_S content, only STDs are created and no DTDs. The maximum Cs solubility in Si at the melting temperature is about 4 to $5x10^{17}$ cm^{-3}. Such C concentration allows to obtain a STD concentration of about $2x10^{15}$ cm^{-3} by annealing (10). This is insufficient for n-p junction creation. A higher concentration of C can, however, be introduced by ion implantation and allows to obtain a much higher STD concentration by thermal annealing (11). This higher STD concentration is sufficient for use in devices, in particular for n-p junctions for solar energy conversion.

In the present paper, a low thermal budget method to form shallow n-p junctions in p-type Cz-Si wafers is presented, based on the enhanced formation of STDs by C ion ion implantation. Such approach can be used for different applications, in particular, for the manufacturing of photoconverters, as the low thermal budget does not lead to

lifetime degradation of non-equilibrium charge carriers. It is possible to introduce C atoms into the near subsurface layer of the silicon substrate with a wide range of concentrations, and to create n-p junctions in the p-Si substrate. Taking into account the low C diffusion coefficient in Si and also the low temperature of C/O related STD formation, it is also possible to form shallow n-p junctions (< 100 nm) by means of C ion implantation.

Experimental

B doped, 10 Ohmcm, (100) p-Si Cz-wafers are used with O and C concentrations of 8 $x10^{17}$ cm^{-3} and $1x10^{17}$ cm^{-3}, respectively, according to the wafers specifications. After standard cleaning of the wafer surface, the wafers are C ion implanted with an energy of 20 keV and C doses between $6.0x10^{11}$ and $1.3x10^{15}$ cm^{-2}. After implantation, thermal annealing is performed in Ar ambient at temperatures between 550 and 750 °C for times ranging between 20 and 300 minutes. The electrical properties of the obtained structures are investigated by the admittance method. This method allows to obtain information on the concentration and position of the levels in the band gap that are responsible for the observed frequency dependence of the measured capacitance. To measure the current-voltage characteristics diode structures were prepared with an area of 0.1 cm^2. Information on the type, size and concentration of structural defects is obtained using X-ray diffraction and diffuse scattering and transmission electron microscopy (TEM).

Results and Discussion

Figure 1 shows the dose dependence of the STD concentration obtained from measurements of the surface conductivity using the 4 point-probe method on 20 keV C ion implanted samples, annealed at different temperatures.

It should be noted that we measure surface resistance in a quite thin (≈ 80 nm) n-type layer and that the possible change of carrier mobility in this layer is not taken into account. The decrease in the conductivity of the doped layer can also be affected by SiO_2 and SiC precipitate formation in the layer during annealing, especially in the samples with a high dose of C ion implantation. This can influence the correct determination of the concentration of electrons, so that the values shown in Figure 1 should be viewed as an estimate. As shown in Figure 1, the concentration of electrons in the doped layer depends on the implantation dose D and the annealing temperature. Effective STD formation takes place at annealing temperatures between 600 and 650 °C. The maximum STD concentration of $7x10^{17}$ cm^{-3}, was obtained for D = $7.5x10^{13}$ cm^{-2} and an annealing temperature of 600 °C. For these conditions, also the best forward and reverse current values have been obtained. The breakdown voltage was typically 60 to 80 V with a maximum value of 150 V for samples with C ion implantation dose of 1.2×10^{14} cm^{-2} and annealed at 650 °C.

At temperatures below 550 °C, no STD formation was observed for all C ion implantation doses. After annealing at 750 °C and for C ion doses above $1.5x10^{13}$ cm^{-2}, a decrease of the conductivity of the implanted layer is observed, which is probably associated with the formation of SiO_2 and SiC precipitates and not with STD formation.

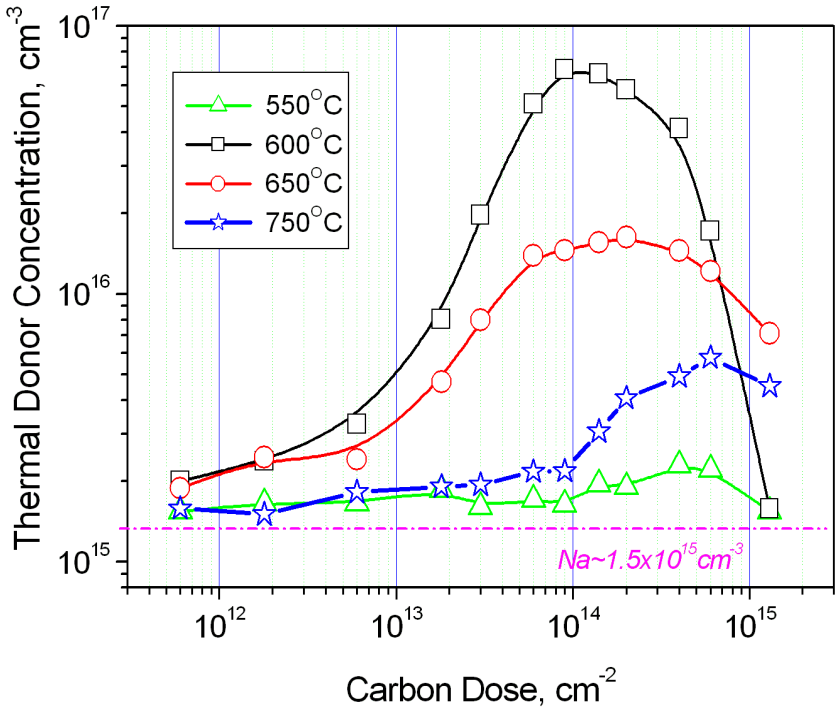


Figure 1. C ion dose dependence of STD concentration after annealing at different temperatures.

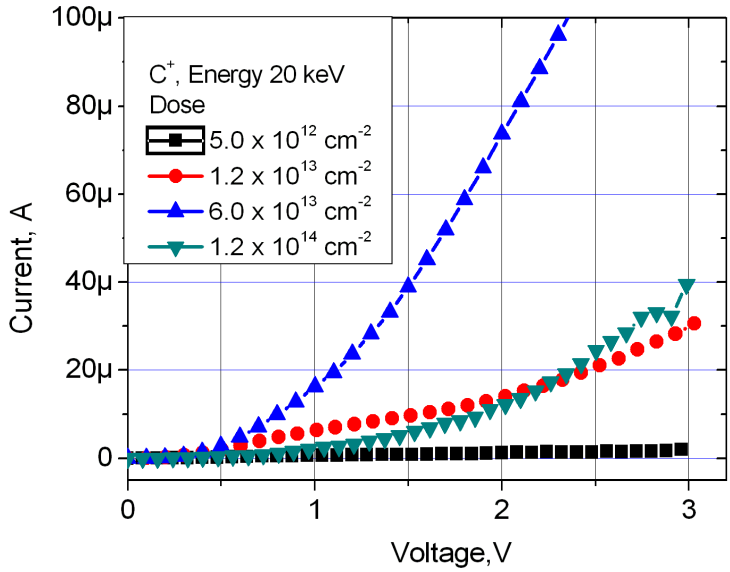
Current-Voltage (I-V) characteristics of the asymmetrical p-n-p structures are shown in Figure 2 (a,b). The reverse currents are quite small and do not exceed 10^{-10} A/cm^2 for a reverse bias of 20 V in the case of a C ion dose 6x10^{13} cm^{-2}. The breakdown voltages of the diode structures are in the range between 60 and 80 V.

For D larger than 5x10^{12} cm^{-2}, an exponential increase of the forward current is observed. The forward current increases with increasing C ion dose up to (0.6-1)x10^{14} cm^{-2}. For D larger than 1×10^{14} cm^{-2}, a decrease of the forward current and an increase of the reverse current are observed. The I-V characteristics asymmetry indicates different barrier values for the p-n and n-p junctions.

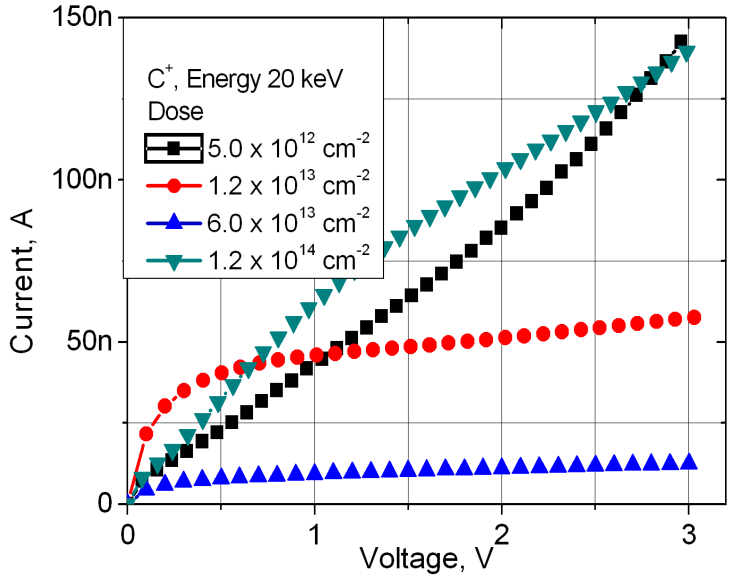
I-V characteristics measured using a voltage sweep frequency of 50 Hz are shown in Figure 2 (c, d) for C ion implantation doses of 2×10^{14} and 6×10^{14} cm^{-2}. A complex shape and hysteresis in case of forward bias are observed when applying a pulsed voltage. This effect is associated with charge carriers capture and release processes at traps due to defect complexes in the near surface region. For voltages between 1 and 2 V, a negative differential resistance area is observed. For a C ion implantation dose exceeding 5x10^{14} cm^{-2}, s-shaped characteristics are observed as illustrated in Figure 2d.

Depth profiles of the C concentration calculated with SRIM 2008 (12) are shown in Figure 3 for different C ion implantation doses. Also shown is the C concentration needed for n-p junction formation in substrates with an acceptor concentration of 1x10^{15} cm^{-3}. As one can see from this figure, a buried n-layer is formed by the C implantation and subsequent anneal, and the diode structure therefor consists of two junctions, a p-n junction at the top of the buried layer and a n-p junction at the bottom.

(a)



(b)



(c) (d)

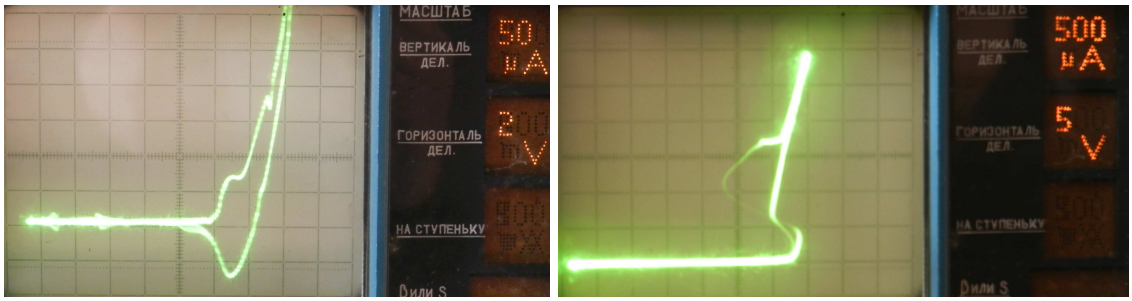


Figure 2. Current-Voltage characteristics of the diode structures formed by C ion implantation: (a) forward bias; (b) reverse bias (b); measurements using pulsed mode voltage for C doses of $2x10^{14}$ cm^{-2} (c) and $6x10^{14}$ cm^{-2} (d).

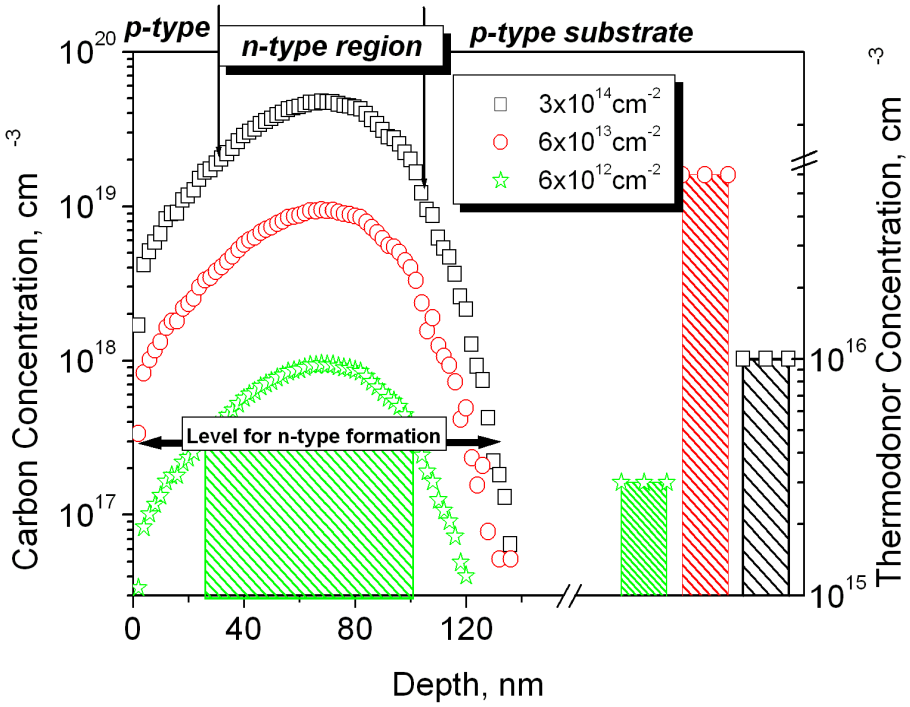


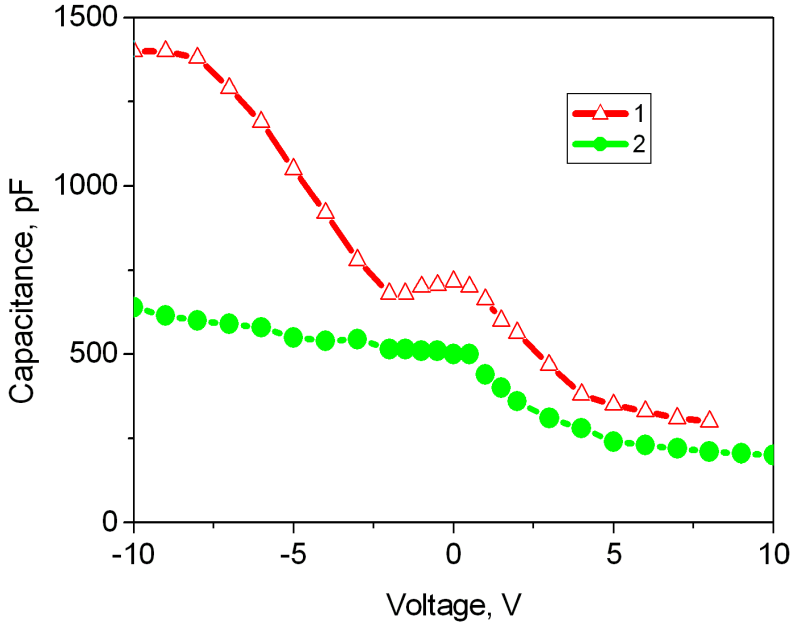
Figure 3. Calculated C depth profiles for three C ion implantation doses, and the corresponding TD concentration.

Due to the presence of two junctions, the I-V characteristics are quite complicated. Also complex is the current transport under different polarity of applied voltage. The complexity of the nature of these processes requires a further detailed study. Further more, n-p structures were obtained using chemical etching to remove the p-type surface layer to a depth of about 50 nm. The current-voltage characteristics of these samples were not yet characterized in detail and results will be published elsewhere (13).

Figure 4 shows the Capacitance - Voltage (C-V) characteristics of a diode, measured at room temperature using a frequency of 1MHz. For a positive voltage applied to the top electrode, a decrease of the capacitance is observed, which is associated with the formation of a space charge region at the n-p junction reverse bias. The area of electronic conductivity (n-region) of the structure is formed by generation of the thermal donors stimulated by C implantation.

For a negative voltage on the electrode, when the n-p junction is biased in the forward direction, a pronounced maximum is observed in the C-V curve. With further increase of negative voltage, the capacitance increases and reaches saturation for a forward bias of 10 to 12 V. The increase in negative voltage removes electrons from the n-region, and a region enriched by holes begins to form. After removal of electrons from the near-surface region, positively charged donor centers remain there. At compensation of this charge by the applied negative voltage, a band bending in the surface region occurs. This leads to the enrichment of this area with holes and the capacitance approaches a value characteristic for a near-surface dielectric. Within the applied voltage interval of -2 to 0 V, in which there is a capacitance peak, the capacitance itself depends on the surface band bending, determined by the applied voltage and the total charge which consists of charge embedded in the dielectric layer and the charge of the ionized thermal donors.

(a)



(b)

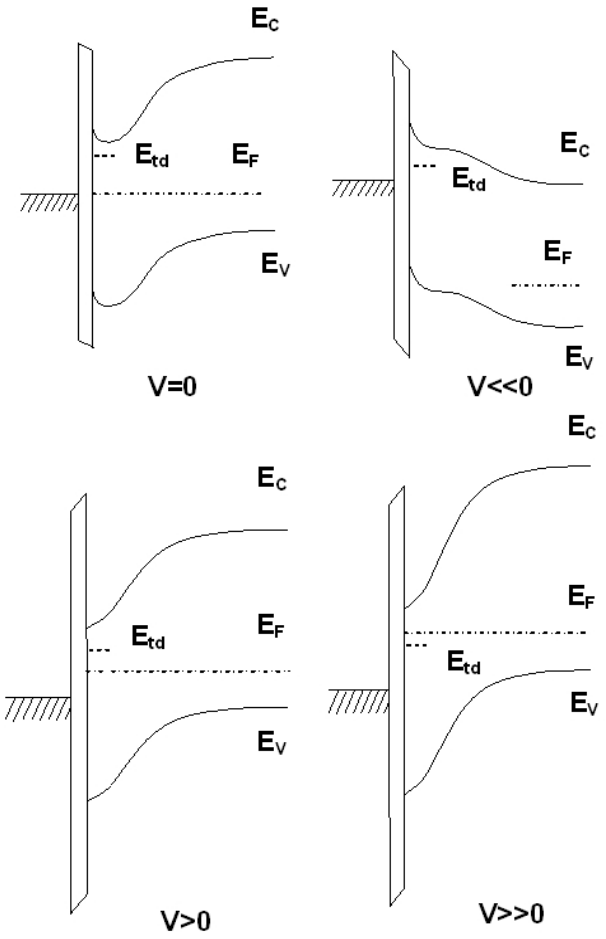


Figure 4. (a) C-V characteristics of a diode structure formed by 20 keV C ion implantation and annealing at 600 °C. Implantation doses are 0.6 (curve 1) and 1.8 10^{14} (curve 2) cm^{-2}. (b) Band diagrams of the structure for different parts of the C-V curves.

A maximum capacitance value is achieved when the Fermi level in the sub-surface region, with increasing applied negative voltage, is close to the middle of the Si band gap. With increasing implantation dose, the TD concentration increases, and at the same time, the thickness of the surface dielectric layer increases by O gettering from the bulk of the wafer to the SiO_2-Si interface (Figure 4, curve 2). Also the density of states at the SiO_2-Si interface increases, which is evident from the changes in the slope of the voltage-capacitance characteristics for the sample implanted by carbon with a dose of 1.8×10^{14} cm^{-2}. Note that near the capacitance peak, a hysteresis is observed in the C-V characteristics under application of positive and negative voltage, indicating the presence of charge capture centers. The band diagrams of these structures at zero, positive and negative voltages are given in Figure 4b, which shows also the band bending.

The dependence of $1/C^2$ for five frequencies of the test signal at room temperature, is shown in Figure 5 illustrating that, for all five curves, the C-V characteristics can be extrapolated by a straight line, intersecting the voltage axis at the potential barrier of the n-p junction yielding a barrier value of approximately 0.64 V.

The temperature dependence of the C-V characteristics is represented in Figure 6 for samples with a dielectric layer between the semiconductor and the metal electrode using a 3 MHz test signal. A clear maximum of the capacitance is observed in the voltage range between - 6 and 3 V. The existence of this maximum in the C-V characteristics shows that there is electric charge storage due to creation of a considerable concentration of STDs in the near surface layer of the p-type substrate.

An analysis of the temperature dependence of the integrated capacitance within the limits of the voltages where this peak exists has been carried out. For that purpose, the peak area under the C-V curve has been calculated using $Ln\left(\int_{V_1}^{V_2} C(V)dV\right) = f\left(\frac{1}{T}\right)$. The obtained dependency of the concentration of electric charge accumulated in the layer with thermal donors is shown in Figure 7 as a function of the inverse temperature. From the Arrhenius plot between 25 °C and 160 °C, an activation energy of 0.012 eV is obtained.

Rocking curves of the (004) X-Ray reflection for the samples implanted with doses of $6x10^{13}$ and $2.5x10^{14}$ C cm^{-2} and annealed at 650 °C, are shown in Figure 8a. There is a mixture of interstitial and vacancy related defects, which lead to local tensile and compressive deformation areas. The defect concentration and stress increase with the C ion implantation dose. The measured mechanical stress values for different implantation doses are listed in Table 1. Tensile stresses are introduced by C_s atoms while compressive stresses are introduced by SiO_x precipitate formation. Increasing the implantation dose leads to a substantial increase of the tensile stresses, whereas the compressive stresses increase more slowly due to the limited availability of O to form SiO_x precipitates.

The distribution of intensity of X-ray diffuse scattering shown by the $\mathbf{q_x}$- curves (Figure 8b) shows that the fields of atomic displacements are nearly spherical. After implantation, the samples are characterized by the presence of a large number of micro-defects both of vacancy and of interstitial type with nearly the same concentration (> 10^{11} cm^{-3}).

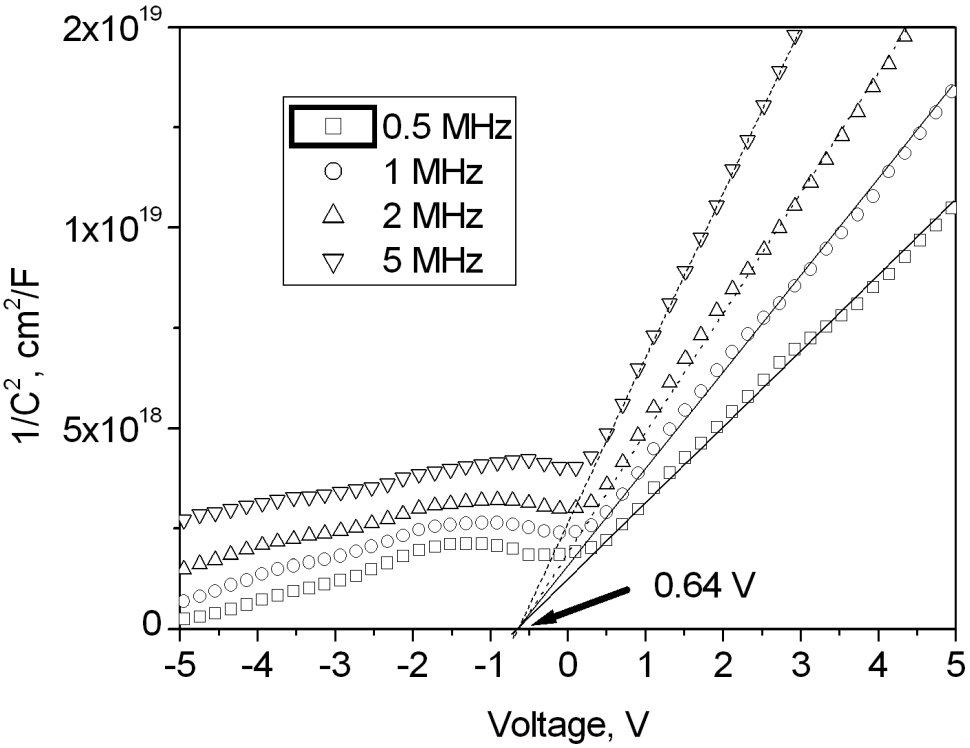


Figure 5. Typical $1/C^2$ dependence on voltage at 300 K.

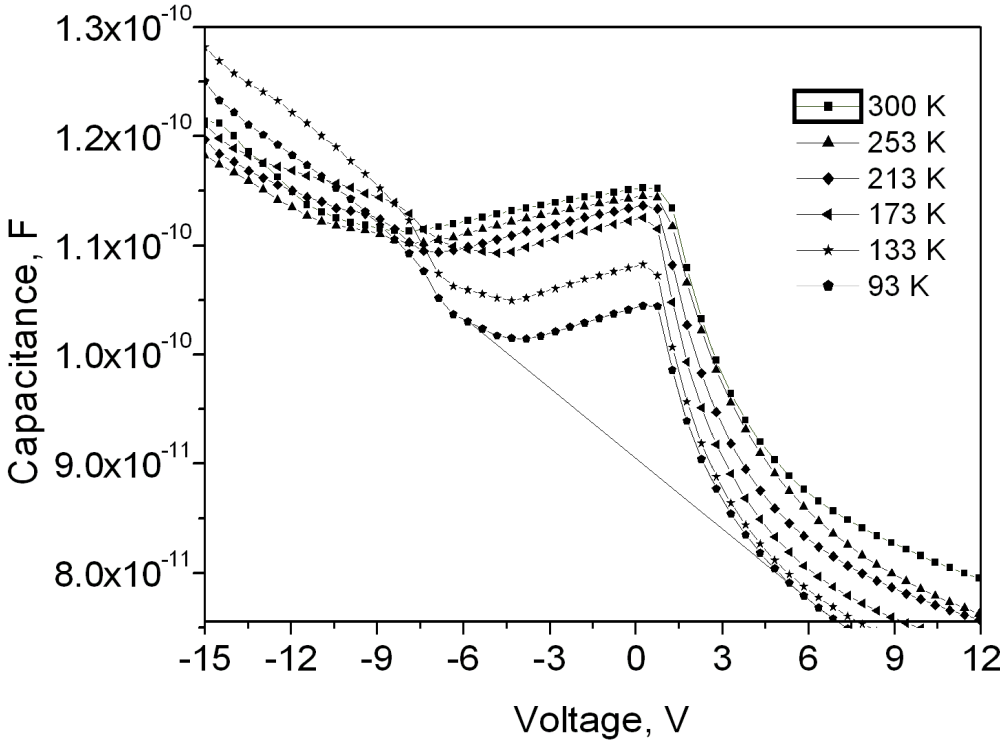


Figure 6. Temperature dependence of capacitance, measured with a 3 MHz test signal.

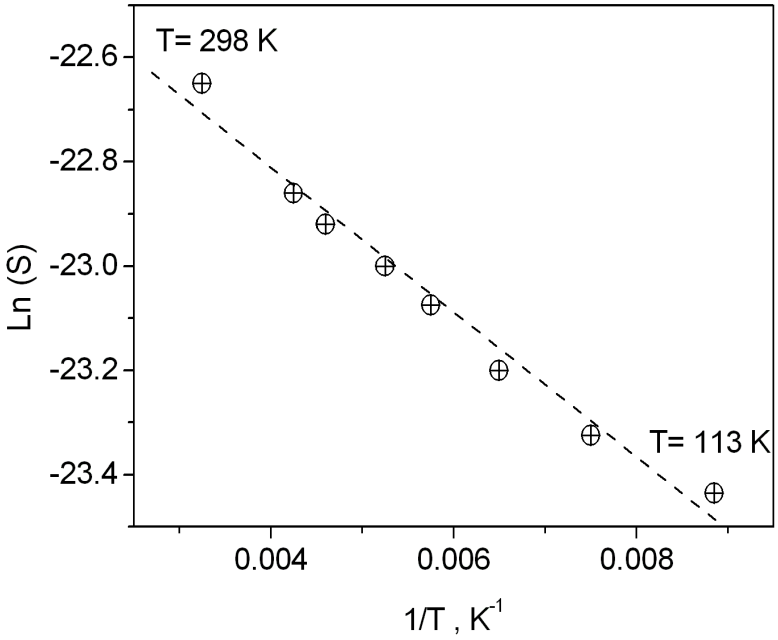


Figure 7. Dependence of the change of the maximum of capacitance area (peak) as a function of the inverse temperature (frequency of capacitance measurements is 3 MHz).

The increase of the intensity in the diffuse scattering curves in the area with large $\mathbf{q}_z$ values on the right of the Bragg maximum observed after annealing between 600 and 700 ^{0}C, indicates the presence of a distribution of interstitial defects smaller than a few tens of nanometers (14). The increase of intensity correlates also with the increase of STD concentration. Figure 8 also shows that after annealing at 650 ^{o}C, the intensity of scattering and thus the concentration of point defects are maximum. After annealing at 750 ^{o}C, the concentration of interstitial defects decreases substantially, and at the same time also that of the STDs. The STDs are related to complexes consisting of self-interstitials and O atoms. The implanted C is a stimulant factor for gettering of O from the bulk of the wafer and for nucleation and growth of STDs. Some of the implanted C atoms become substitutional during the anneal and do no longer diffuse.

Table 1. Mechanical stress for different implantation doses

Dose of C implantation, cm^{-2}	**Tensile deformation**	**Compressive deformation**
1.2x10^{13}	1.2 **x**10^{-4}	4.76x10^{-4}
6.0x10^{13}	2.01x10^{-4}	7.01x10^{-4}
2.5x10^{14}	3.79x10^{-4}	9.30x10^{-4}

Oxygen from the near-surface region partly diffuses to the surface, resulting in a slight increase of the SiO_x film thickness as was also observed after As implantation (15). The final thickness of the oxide film depends on the annealing time and O_i concentration in the thin subsurface layer of the Si substrate. From the implanted C atoms, only C_s participates in STD formation. The concentration of STDs depends on the C_s and Oi concentration in the C ion implanted layer of the substrate. For the annealing temperatures used in the present study, O_i can diffuse rapidly to this region

(16) and can form larger SiO_x complexes without any thermal donor activity. This effect is observed with increasing annealing temperature, which leads also to an increase of the precipitate critical radius (17) and O_i diffusion. At annealing temperatures above 700 °C, only large SiO_x precipitates without donor activity are stable. Some of the implanted C atoms become substitutional during the anneal and do no longer diffuse. Under the influence of the tensile stresses around the C_s atoms, O atoms diffuse into the region with high C concentration during the annealing at temperatures between 600 and 650 °C and STDs are formed. The critical size of the oxygen clusters at low temperature is small, so they are stable.

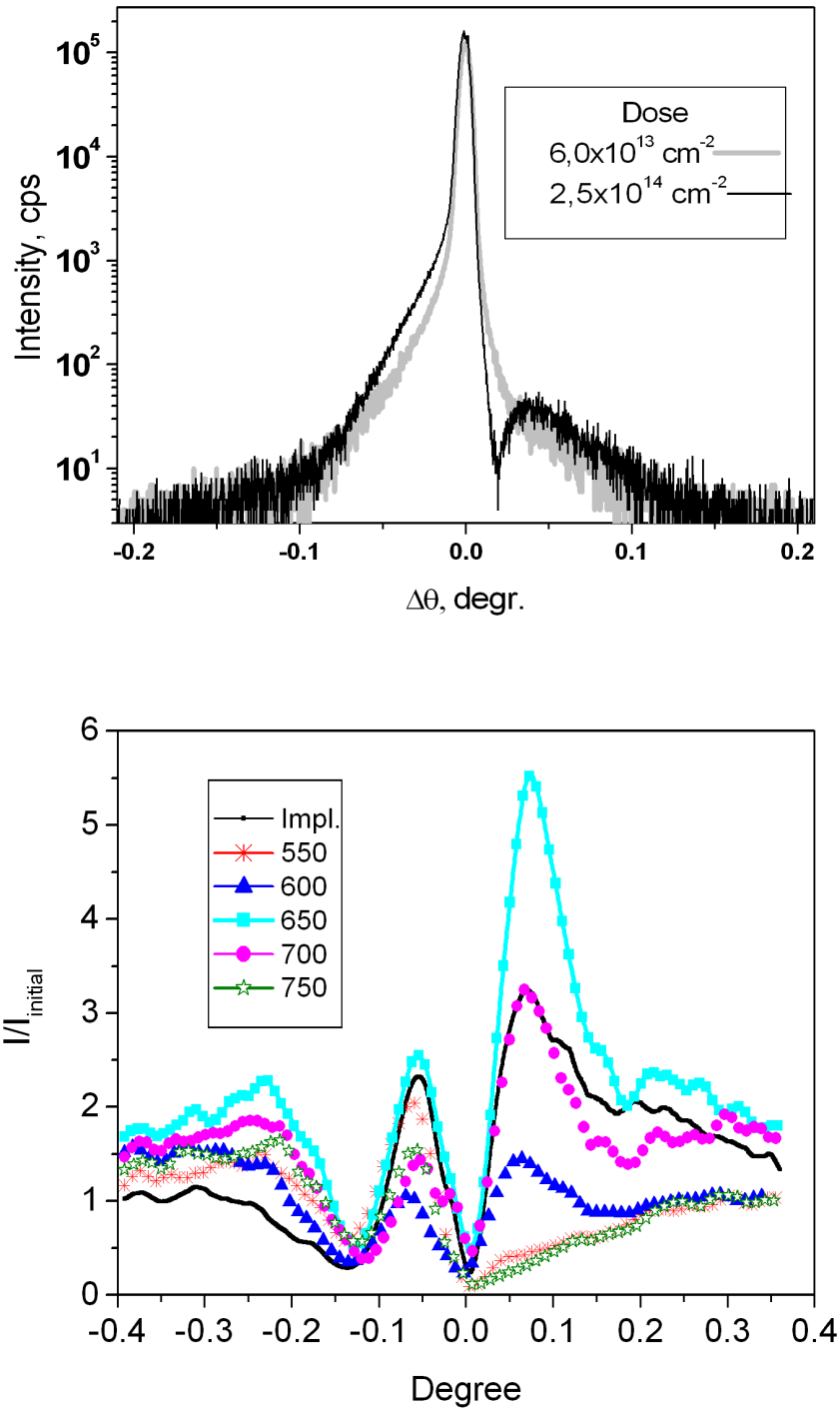


Figure 8. XRD spectra (top) and curves of intensity distribution of X-ray diffuse scattering (bottom) for the C ion implanted samples, annealed at different temperatures.

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A TEM image of a 6.0×10^{13} cm^{-2} C ion implanted Si surface layer after annealing at 600 ^oC, is shown in Figure 9. Defects of two typical sizes are observed: small defects (D1) with a size smaller than 1 nm and larger defects (D2) which are about 2 nm in size. The average distance between the small defects is 30 nm (corresponding with a concentration of about $2\text{-}3\times10^{16}$ cm^{-3}) while the average distance between the larger defects is 70-90 nm. We assume that the smaller defects might be related with thermal donors because their concentrations are similar and correlation is also observed between their concentration changes depending on the annealing conditions and the C ion implantation dose. No small defects were e.g. observed with a concentration greater than 3×10^{15} cm^{-3} in the wafers with low carbon content (dose < 1×10^{13} cm^{-2}) and also not when annealing at temperatures 550 and 750 ^oC for all implantation doses. For these regimes, the thermal donor concentration is indeed also in the range between 1 and 4×10^{15} cm^{-3}. The larger defects have a size and concentration that is typical for the SiO_x precipitates in Si for the used annealing temperatures (18).

As the STD concentration dependence on the C implantation dose shows, only about 10% of the implanted C atoms are involved in STD formation. This dose relationship is nonlinear, and therefor only qualitative data on the TD concentration can be obtained. Additional experiments are needed to clarify and quantify the relation between C ion dose and STD concentration. With increase of implantation dose, the concentration of C related thermal donors increases. When the dose exceeds a certain critical value, however, a competition for O between C_s atoms starts. The lack of sufficient O atoms leads then to a saturation of STD formation.

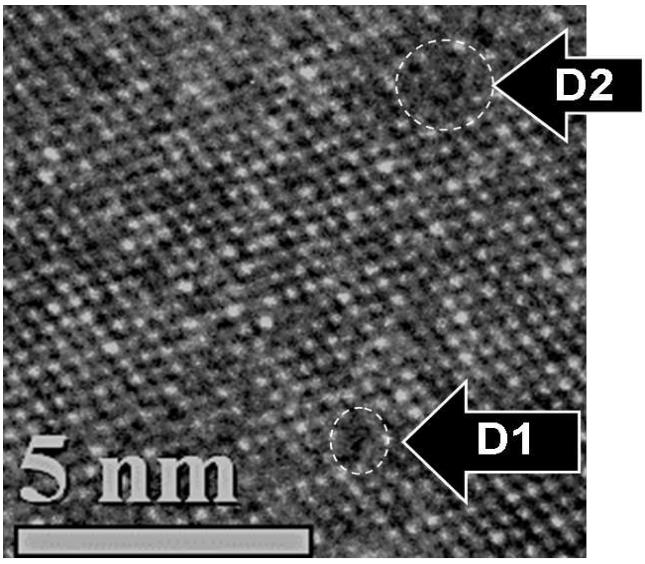

Figure 9. TEM image of $6.0x10^{13}$ cm^{-2} C ion implanted Si surface layer after annealing at 600 ^oC.

Conclusions

It is shown that C ion implantation in p-type Cz-Si and subsequent annealing at temperatures in the range between 600 and 650 °C can reliably and reproducibly create n-p junctions with breakdown voltages of 100 - 150 V. The highest breakdown voltages and the lowest leakage currents are realized for an implantation dose of $1x10^{14}$ cm^{-2} and for annealing at 650 °C. It is shown that the concentration of thermal donors depends on the annealing temperature and the C implantation dose. The maximum thermal donor concentration of about $5x10^{16}$ cm^{-3} is observed after annealing at 650 ºC and a C ion dose of $1x10^{14}$ cm^{-2}. After annealing at 750 ºC, no STDs are observed.

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